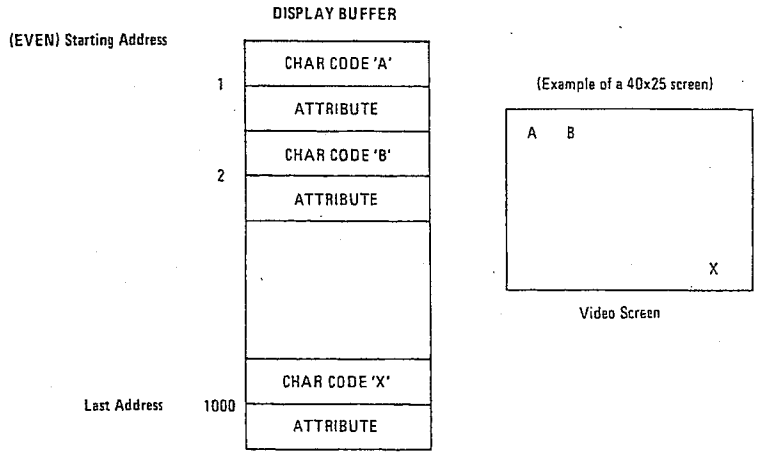
EXHIBIT 6
(PART 2 OF 2)

Description of Basic Operations

In the alphanumeric mode the adapter fetches character and attribute information from its display buffer. The starting address of the display buffer is programmable through the 6845, but it must be an even address. The character codes and attributes are then displayed according to their relative position in the buffer.



The CPU and the display control unit have equal access to the display buffer during all the operating modes except high resolution alphanumeric. During this mode, the CPU should access the display buffer during the vertical retrace time (if not, then the display will be affected with random patterns as the CPU is using the display buffer). The characters are displayed from a prestored "character generator" which contains the dot patterns of all the displayable characters.

In the graphics mode the displayed dots and colors are also fetched from the display buffer (up to 16K bytes). In the Color/Graphics Mode Section, the bit configuration for each graphics mode is explained.

Table 5. Summary of Available Colors

I	R	G	B	COLOR
0	0	0	0	Black
0	0	0	1	Blue
0	0	1	0	Green
0	0	1	1	Cyan
0	1	0	0	Red
0	1	0	1	Magenta
0	1	1	0	Brown
0	1	1	1	Light Gray
1	0	0	0	Dark Gray
1	0	0	1	Light Blue
1	0	1	0	Light Green
1	0	1	1	Light Cyan
1	1	0	0	Light Red
1	1	0	1	Light Magenta
1	1	1	0	Yellow
1	1	1	1	White

Note: "I" provides extra luminance (brightness) to each shade available. Resulting in the light colors listed above, except where the "I" bit is not recognized by some monitors.

Programming Considerations

Programming the 6845 CRT Controller

The 6845 has 19 internal registers which are used to define and control a raster scanned CRT display. One of these registers, the Address Register, is actually used as a pointer to the other 18 registers. It is a write only register which is loaded from the CPU by executing an OUT instruction to I/O address 3D4. The five least significant bits of the I/O bus are loaded into the Address Register.

In order to load any of the other 18 registers, the Address Register is first loaded with the necessary pointer and then the CPU may output a value to I/O address 3D5 in order to load the information in the preselected register.

The following table defines the values which must be loaded in 6845 Registers in order to control the different modes of operation supported by the attachment.

Table 6. 6845 Register Description

ADDR REG.	REG. #	REGISTER TYPE	UNITS	I/O	40x25 ALPHA	80x25 ALPHA	GRAPHIC MODES
0	R0	Horizontal Total	Char.	Write Only	38	71	38
1	R1	Horizontal Displayed	Char.	Write Only	28	50	28
2	R2	Horiz. Sync Position	Char.	Write Only	2D	5A	2D
3	R3	Horiz. Sync Width	Char.	Write Only	0A	0A	0A
4	R4	Vertical Total	Char. Row	Write Only	1F	1F	7F
5	R5	Vertical Total Adjust	Scan Line	Write Only	06	06	06
6	R6	Vertical Displayed	Char. Row	Write Only	19	19	64
7	R7	Vert. Sync Position	Char. Row	Write Only	1C	1C	70
8	R8	Interlace Mode	–	Write Only	02	02	02
9	R9	Max Scan Line Addr.	Scan Line	Write Only	07	07	01
A	R10	Cursor Start	Scan Line	Write Only	06	06	06
B	R11	Cursor End	Scan Line	Write Only	07	07	07
C	R12	Start Addr. (H)	–	Write Only	00	00	00
D	R13	Start Addr. (L)	–	Write Only	00	00	00
E	R14	Cursor Addr. (H)	–	Read/ Write	XX	XX	XX
F	R15	Cursor Addr. (L)	–	Read/ Write	XX	XX	XX
10	R16	Light Pen (H)	–	Read Only	XX	XX	XX
11	R17	Light Pen (L)	–	Read Only	XX	XX	XX

Note: All register values are given in hexadecimal.

Programming the Mode Control and Status Register

The following I/O devices are defined on the Color/Graphics Adapter.

HEX ADDR.	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	FUNCTION OF REGISTER
X'3D8'	1	1	1	1	0	1	1	0	0	0	DO REG (MODE CONTROL)
X'3D9'	1	1	1	1	0	1	1	0	0	1	DO REG (COLOR SELECT)
X'3DA'	1	1	1	1	0	1	1	0	1	0	DI REG (STATUS)
X'3DB'	1	1	1	1	0	1	1	0	1	1	CLEAR LIGHT PEN LATCH
X'3DC'	1	1	1	1	0	1	1	1	0	0	PRE SET LIGHT PEN LATCH
X'3D0'	1	1	1	1	0	1	0	Z	Z	0	6845 REGISTERS
X'3D1'	1	1	1	1	0	1	0	Z	Z	1	6845 REGISTERS
X'3D0'	1	1	1	1	0	1	0	Z	Z	0	6845 REGISTERS
X'3D1'	1	1	1	1	0	1	0	Z	Z	1	6845 REGISTERS

Z = don't care condition

HARDWARE

Color Select Register

This is a 6 bit output only, register, it can not be read, its address is X'3D9' and can be written using the 8088 I/O OUT command.

The following is a description of the Register functions.

Bit 0	B (BLUE) Border Color Select ALPHA/BACKGROUND
Bit 1	G (GREEN) Border Color Select ALPHA/BACKGROUND
Bit 2	R (RED) Border Color Select ALPHA/BACKGROUND
Bit 3	I Intensifies Border Color Select ALPHA/BACKGROUND IN 320 x 200
Bit 4	Select Alt Back Color Set For Alpha Color Modes
Bit 5	320 x 200 Color Set Select
Bit 6	Not Used
Bit 7	Not Used

Bits 0, 1, 2, 3. Select the screens border color in 40x25 alpha mode. In graphics mode (medium resolution) 320 x 200 color, the screen background color (C0-C1) is selected by these bit settings.

Bit 4. This bit when set will select on alternate, intensified, set of background colors in the alpha mode.

Bit 5 is only used in the medium resolution color mode (320 x 200). It is used to select the active set of screen colors for the display.

When bit 5 is set to a "1" colors are determined as follows.

The	C1	C0	Set selected are:
	0	0	Background as defined by Bit 0-3 of Port '3D9'
	0	1	Cyan
	1	0	Magenta
	1	1	White

When bit 5 is set to a "0" Colors are determined as follows.

The	C0	C1	Set selected are:
	0	0	Background as defined by Bit 0-3 of Port '3D9'
	0	1	Green
	1	0	Red
	1	0	Yellow

Mode Select Register

This is a 6 bit output only register, it can not be read. Its address is X'3D8'. It can be written using the 8088 I/O OUT command.

The following is a description of the registers functions.

Bit 0

Bit 0	80 x 25 mode
Bit 1	Graphic Select
Bit 2	B & W Select
Bit 3	Enable Video Signal
Bit 4	High Res 640 x 200 B & W Mode
Bit 5	Change BACKGROUND INTENSITY to Blink Bit
Bit 6	Not Used
Bit 7	Not Used

Bit 0 Selects between 40 x 25 and 80 x 25 alpha mode, a "1" sets it to 80 x 25 mode.

Bit 1 Selects between ALPHA mode and 320 x 200 graphics mode, a "1" select 320 x 200 graphics mode.

Bit 2 Selects color or B & W mode, a "1" selects B & W.

Bit 3 Enables the video signal at certain times when modes are being changed. The video signal should be disabled when changing modes. A "1" enables the video signal.

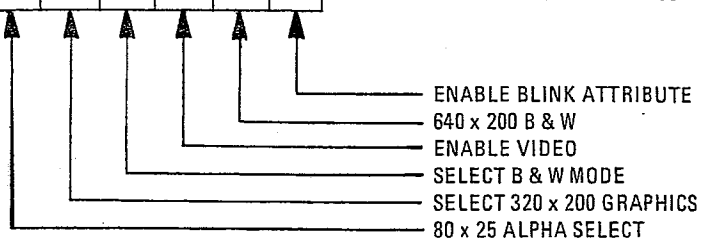
Bit 4 When on, this bit selects the 640 x 200 B & W graphics mode. One color of 8 can be selected on direct drive sets in this mode by using register 3D9.

Bit 5 When on, this bit will change the character background intensity to the blinking attribute function for ALPHA modes. When the high order attribute bit is not selected, 16 background colors (or intensified colors) are available. For normal operation, this bit should be set to "1" to allow the blinking function.

Mode Register Summary

Bits

0	1	2	3	4	5	
0	0	1	1	0	1	40 x 25 ALPHA B & W
0	0	0	1	0	1	40 x 25 ALPHA COLOR
1	0	1	1	0	1	80 x 25 ALPHA B & W
1	0	0	1	0	1	80 x 25 ALPHA COLOR
0	1	1	1	0	z	320 x 200 B & W GRAPHICS
0	1	0	1	0	z	320 x 200 COLOR GRAPHICS
0	1	1	1	1	z	640 x 200 B & W GRAPHICS



z = don't care condition

* THE LOW RESOLUTION 160 x 100 MODE REQUIRES SPECIAL PROGRAMMING AND IS SET UP AS ALPHA MODE 40 x 25

Status Register

The status register is a 4 bit read only register. Its address is X'3DA'. It can be read using the 8088 I/O IN instruction.

The following is a description of the register functions.

Bit 0 Display Enable
Bit 1 Light Pen Trigger Set
Bit 2 Light Pen SW Made
Bit 3 Alpha Dots
Bit 4 Not Used
Bit 5 Not Used
Bit 6 Not Used
Bit 7 Not Used

Bit 0 This input bit, when active, indicates that a regen buffer memory access can be made without interfering with the Display.

Bit 1 This bit, when active, indicates that a positive going edge from the light pen input has set the light pen trigger. This trigger is reset on power on and may also be cleared by doing an I/O OUT command to address X'3DB'. No specific data setting is required, the action is address activated.

Bit 2 The light pen switch status is reflected in this status bit. The switch is not latched or debounced. A "0" indicates the switch is on.

Bit 3 The ALPHA video output signal is readable in this status bit. Its purpose is to verify that video information is being generated for RAS purposes.

Sequence of Events

1. Determine mode of operation
2. Reset Video Enable bit
3. Program 6845 to select mode
4. Program mode/color select registers

Memory Requirements

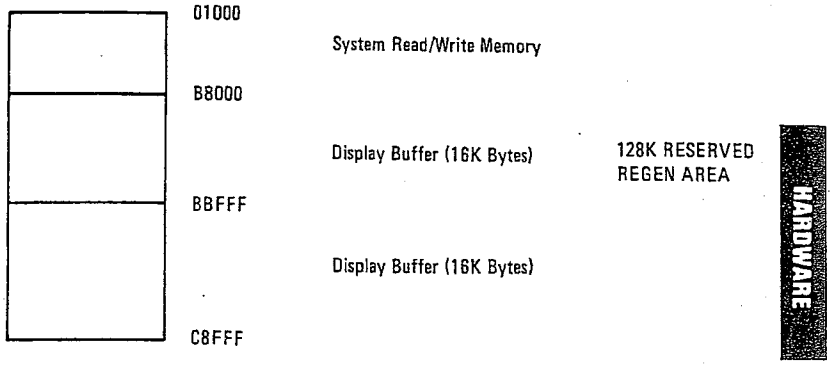
The memory used by this adapter is self-contained. It consists of 16k bytes of memory without parity. This memory is used as both a display buffer for alphanumeric data and as a bit map for graphics data. The Regen Buffers address starts at X'B8000'.

Interrupt Level (Vertical Retrace)

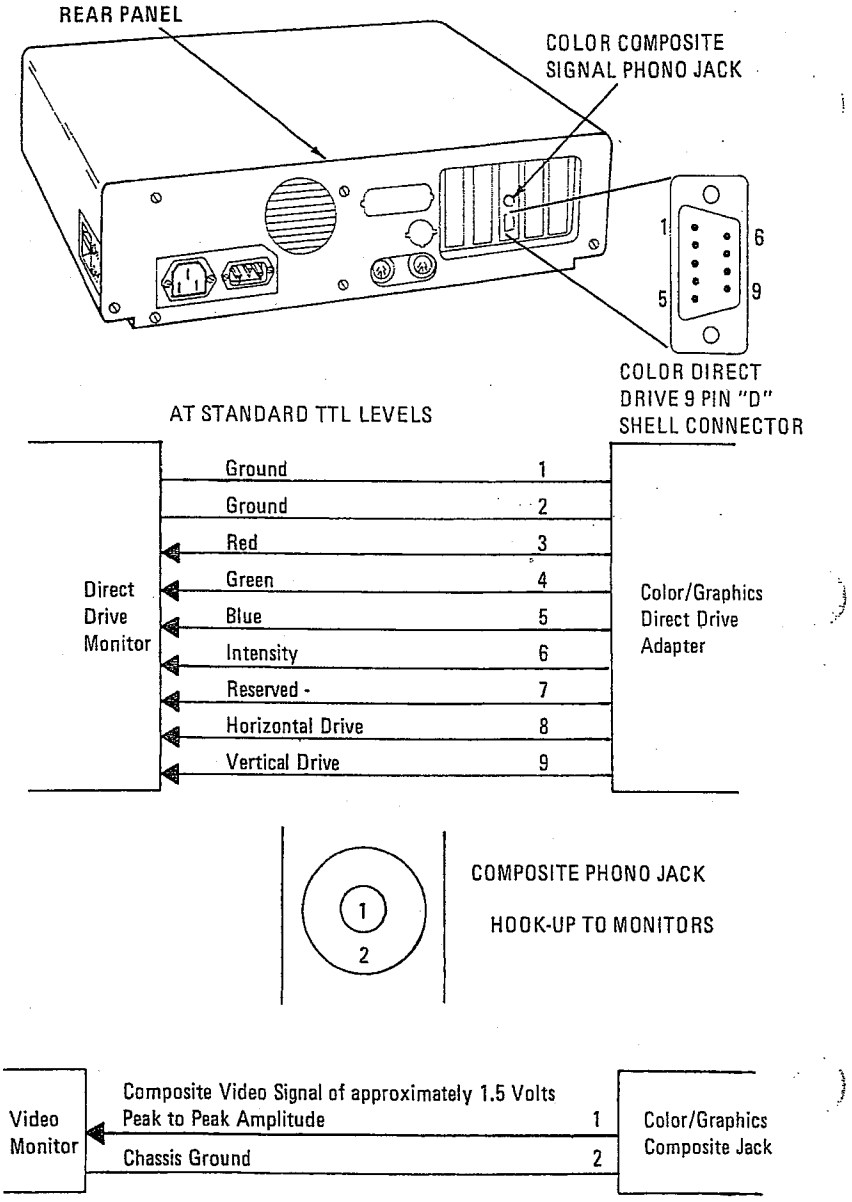
Level 2

I/O Address and Bit Map

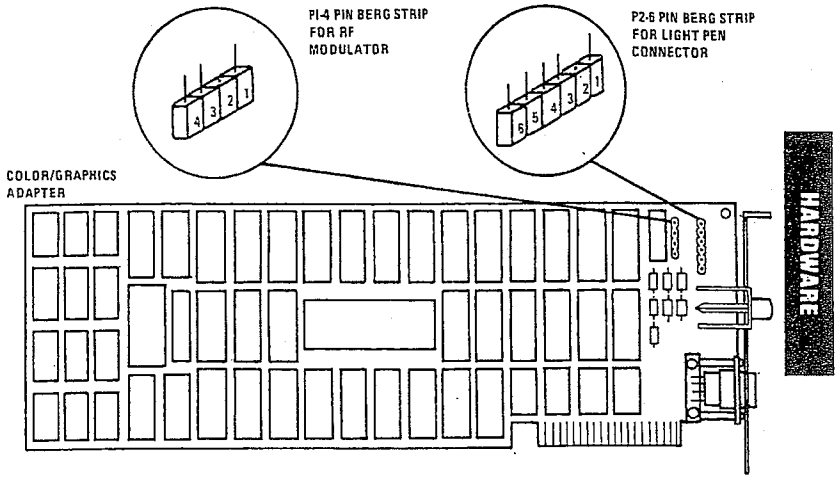
Read/Write Memory Address Space

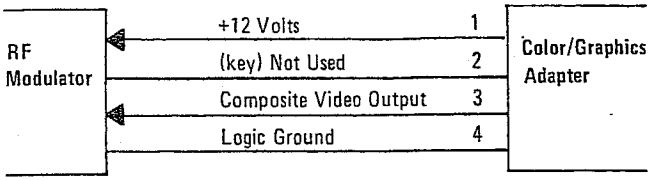


Color/Graphics Monitor Adapter Direct Drive, and Composite Interface Pin Assignment

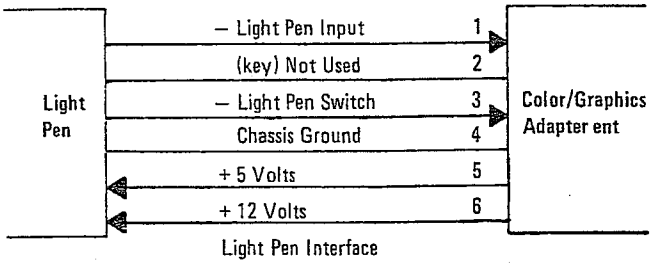


Color/Graphics Monitor Adapter
Auxiliary Video Connectors





RF Modulator Interface



Light Pen Interface

GLOSSARY

1. Address Buss: A set of wires or signals carrying the binary-coded address from the Intel-8088 microprocessor throughout the rest of the IBM Personal Computer System Unit.
2. AEN: Address Enable. (Refer to System Board I/O Channel Descriptions).
3. ALE: Address Latch Enable. (Refer to System Board I/O Channel Descriptions).
4. Analog: (1) Pertaining to representation by means of continuously variable physical quantities. (2) Contrast with digital.
5. A/N: Alphanumeric: Pertaining to a character set that contains letters, digits, and usually other characters, such as punctuation marks. Syonymous with alphameric.
6. A0-A19: Address bits 0-19. (Refer to System Board I/O Channel Descriptions).
7. APA: All points addressable graphics.
8. ASCII: American Standard Code of Information Interchange. The standard code, using a coded character set consisting of 7-bit coded characters (8 bits including parity check), used for information interchange among data processing systems, data communication systems and associated equipment. The ASCII set consists of control characters and graphic characters.
9. Assembler: A computer program used to assemble. Synonymous with assembly program.
10. BASIC: (Beginner's all-purpose symbolic instruction code). A programming language with a small repetoire of commands and a simple syntax, primarily designed for numerical application.
11. BAUD: (1) A unit of signaling speed equal to the number of discrete conditions or signal events per second in Morse code, one bit per second in a train of binary signals, and one 3-bit value per second in a train of signals each of which can assume one of eight different states. (2) In asynchronous transmission, the unit of modulation rate corresponding to one unit of interval per second, i.e. if the duration of the unit interval is 20 milliseconds, the modulation rate is 50 baud.

12. Binary: (1) Pertaining to a selection, choice, or condition that that has two possible values or states. (2) Pertaining to a fixed radix numeration system having a radix of two.
13. BIOS: Basic Input/Output System.
14. Bootstrap: A technique or device designed to bring itself into a desired state by means of it's own action, e.g. a machine routine whose first few instructions are sufficient to bring the rest of itself into the computer from an input device.
15. Buffer: An area of storage that is temporarily reserved for use in performing an input/output operation, into which data is read or from which data is written. Synonymous with I/O area. A portion of storage for temporarily holding input or output data.
16. Bus: One or more conductors used for transmitting signals or power.
17. Byte: (1) A binary character operated upon as a unit and usually shorter than a computer word. (2) The representation of a character.
18. CLK: Clock. (Refer to System Board I/O Channel Descriptions).
19. Code: (1) A set of unambiguous rules specifying the manner in which data may be represented in a discrete form. Synonymous with coding scheme. (2) A set of items such as abbreviations representing the members of another set. (3) Loosely, one or more computer programs, or part of a computer program. (4) To represent data or a computer program in a symbolic form that can be accepted by a data processor.
20. Computer: A data processor that can perform substantial computation, including numerous arithmetic operations, or logic operations, without intervention by a human operator during the run.
21. CPS: Characters per second.
22. CRC: The cyclic redundancy check character.
23. CRT: (1) A Cathode ray tube display. (2) A display device, such as the IBM Monochrome Display, that uses a cathode ray tube.
24. CTS: Conversational Terminal System. (2) Clear to Send. Associated with modem control.
25. DACK0-DACK3: DMA Acknowledge 0 to 3. (Refer to System Board I/O Channel Description).

26. Data: (1) A representation of facts, concepts or instructions in a formalized manner suitable for communication, interpretation, or processing by humans or automatic means. (2) Any representations such as characters or analog quantities to which meaning is, or might be assigned.
27. Din Connectors: One of the connectors specified by the Din standardization committee.
28. DIP: "Dual In-Line Package." A widely used container for an integrated circuit. DIP's are pins usually in two parallel rows. These pins are spaced on 1/10" inters and come in different configurations ranging from a 14-pin assembly to a 40-pin configuration.
29. Display: A visual presentation of data.
30. DMA: Direct Memory Access.
31. DO-D7: Data Bits 0 to 7. (Refer to System Board I/O Channel Descriptions).
32. DRQ1-DRQ3: DMA Request 1 to 3. (Refer to System Board I/O Channel Descriptions).
33. DSR: Data Set Ready, associated with modem control.
34. DTR: Distribution Tape Reel.
35. Edge Connector: An opening which joins with the end of a circuit board. The purpose of this interface is to send electrical signals back and forth.
36. EIA/CCITT Drives: Electronic Industries Association/ Consultative Committee on International Telegraphy and Telephony Drives.
    EPROM or 'PROM': Term for "Programmable Read-Only Memory." An EPROM or 'PROM' is actually Read-Only Memory (ROM) but the contents may be changed by electrical means. EPROM or 'PROM' information is not destroyed when the power is cut off.
37. Firmware: Memory chips with the software programs already built in.
38. Graphics: Symbols Produced by a process such as handwriting, drawing or printing. Synonymous with graphic symbol.
39. Hexadecimal: Pertaining to a selection, choice, or condition that has sixteen possible values or states. These values or states usually contain 10 digits and six letters A through F. Hexadecimal digits are equivalent to a power of 16.

40. Hertz (Hz.): A unit of frequency equal to one cycle per second.
41. High order position: The leftmost position in a string of characters.
42. Input/Output (I/O): Pertaining to a device or to a channel that may be involved in an input process, and, at a different time, in an output process. (2) Pertaining to a device whose parts can be performing an input process and an output process at the same time.
43. Integrated Circuit: A combination of interconnected circuit elements inseperably associated on or within a continuous substrate.
44. Interpreter: A computer program used to interpret. Synonymous with interpretive program.
45. Interrupt: (1) A suspension of a process, such as the execution of a computer program, in such a way that the process can be resumed. (2) To stop a process in such a way that it can be resumed. (3) In data transmission, to take an action at a receiving station that causes the transmitting station to terminate a transmission.
46. I/O Channel: Input/Output Channel. In a data processing system, a functional unit, controlled by the processing unit, that handles the transfer of data between main storage and peripheral equipment.
47. I/O CH CK: I/O Channel Check. (Refer to System Board I/O Channel Descriptions).
48. I/O CH RDY: I/O Channel Ready. (Refer to System Board I/O Channel Descriptions).
49. IMR: Interruption Mask Register.
50. IOR: I/O Read Command. (Refer to System Board I/O Channel Descriptions).
51. IOW: I/O Write Command: (Refer to System Board I/O Channel Descriptions).
52. IRQ2-IRQ7: Interrupt Request 2 to 7. (Refer to System Board I/O Channel Descriptions).
53. K: An abbreviation for the prefix kilo, i.e. 1000 in decimal notation. To the tenth power, 1024 in decimal notation.
54. KB: Kilobyte.
55. Khz: Kilohertz. A unit of frequency equal to 1,000 hertz.

56. Low order position: The rightmost position in a string of characters.

57. Machine Language: (1) A language that is used directly by a machine. (2) Another term for computer instruction code.

58. Memory Address: A two-byte value selecting one specific memory location on a memory map.

59. Memory Location: The most specific part of a memory map that the computer can refer to.

60. Memory Map: The list of memory locations addressed directly by the microprocessor.

61. MEMR: Memory Read Command. (Refer to System Board I/O Channel Descriptions).

62. MEMW: Memory Write Command. (Refer to System Board I/O Channel Descriptions).

63. MFM Coded: Modified Frequency Modulation. It is double density encoding of information on a diskette.

64. Mhz: Megahertz. A unit of frequency equal to one million Hertz.

65. Microprocessor: A processing unit, or part of a processing unit, that consists of microcode. In the IBM Personal Computer, the microprocessor is the Intel-8088.

66. Mnemonic: Symbol or symbols used instead of terminology more difficult to remember. Usually a mnemonic has two or three letters.

67. Mode: (1) A method of operation; for example, the binary mode, the interpretive mode, the alphanumeric mode. (2) The most frequent value in the statistical sense.

68. Monitor: (1) A device that observes and verifies the operation of a data processing system and indicates any specific departure from the norm. (2) A television type display such as the IBM Monochrome Display. (3) Software or hardware that observes, supervises, controls, or verifies the operations of a system.

69. Multiplexer: A device capable of interleaving the events of two or more activities or capable of distributing the events of an interleaved sequence to their respective activities.

70. OR: A logic operator having the property that if P is a statement, Q is a statement, R is a statement..., then the OR of P,Q,R, is true if at least one statement is true, false if all statements are false. P OR Q is often represented by P+Q, PVQ. The term is synonymous with boolean add; logic add.
71. "ORed": Past tense of OR.
72. OSC: Oscillator. (Refer to System Board I/O Channel Descriptions).
73. Output: Pertaininng to a device, process, or channel involved in an output process, or to the data or states involved in an output process.
74. Personal Computer: A small home or business computer complete with a System Unit, keyboard, and available with a variety of options such as monochrome display and a dot matrix printer.
75. Pinout: A diagram of functioning pins on a pinboard.
76. Printed Circuit Board: A piece of material, usually fiberglass, which contains a layer of conductive material, usually metal. The metallic layer is then etched and electronic equipment is then attached to the fiberglass. The electronic equipment then has the capacity to transmit electronic signals through the board by way of the etched metal tracks.
77. Program: (1) A series of actions designed to achieve a certain result. (2) To design, write and test computer programs.
78. Read/Write Memory: Random access storage.
79. Reset Drv: Reset Driver. (Refer to System Board I/O Channel Descriptions).
80. RF Modulator: The device used to convert the composite video signal to the antenna level input of a home TV.
81. ROM: Read-only Memory.
82. ROM BIOS: Read-only Memory/Basic Input Output System.
83. RS 232 Port: Asynchronous Type Communications.
84. RTS: Ready to Send. Associated with modem control.

85. Scan Line: The use of a cathode beam to test the cathode ray tube of a display used with a personal computer.

86. Schematic: The description, usually in diagram form, of the logical structure and physical structure of an entire data base according to a conceptual model.

87. Software: (1) Computer programs, procedures, rules, and possibly associated documentation concerned with the operation of a data processing system. (2) Contrast with hardware.

88. Strobe: (1) An instrument used to determine the exact speed of circular or cyclic movement. (2) A flashing signal displaying an exact event.

89. Text: In ASCII and data communication, a sequence of characters treated as an entity if preceded and terminated by one STX and one ETX transmission control respectively.

90. TX Data: Transmit Data. External connections of the RS 232 Asynchronous Communications Adapter interface.

91. Video: Computer data shown or displayed on a cathode ray tube monitor or display.